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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,751	11/21/2002	Neal Margulis	MA74-012	5804

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WELLS ST. JOHN ROBERTS GREGORY & MATKIN P.S.
601 W. FIRST AVENUE
SUITE 1300
SPOKANE, WA 99201-3828

EXAMINER
CHAUHAN, ULKA J

ART UNIT	PAPER NUMBER
2676	4

DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,751	MARGULIS, NEAL	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Preliminary Amendment

1. Claims 1-33 are cancelled. Newly added claims 34-43 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 34, 36, 38-41, and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,247,084 to Apostol, Jr., et al.

5. As per claims 34 and 40, Apostol teaches an integrated circuit 10 having a unified memory architecture ("a common display memory and main memory") includes processor 12 ("(CPU) subsystem controller"); memory controller 14 ("a memory controller"); plurality of bus transactor circuits 15A-15C comprising dual port RAMs 122A-C ("internal memory subsystem"), graphics and display subsystem 126C ("a graphics/drawing and display subsystem"), and PCI and parallel I/O subsystem ("a peripheral bus controller"); shared memory

port 20; and dual system buses 22 and 24 at Fig. 1, col. 4 lines 29-37 and col. 6 lines 50-67. The memory controller 14 is coupled to shared memory port 20 which is coupled to an external memory device 46 ("external memory subsystem"), which can include a synchronous dynamic random access memory (SDRAM), col. 4 lines 38-45. System bus 22 ("multi-use memory channel") is a data bus which carries memory data being transmitted to and from external memory 46 by bus transactor circuits 15A-15C and processor 12 through memory controller 14, col. 4 lines 51-54. Apostol further discloses that the memory controller 14 includes an internal command and data bus arbiter 272 for arbitrating accesses to the command and data buses and the memory controller 14 asserts a 3-bit data grant output to indicate which subsystem should drive data on to data bus 22 on the following clock for DMA data transfers to external memory 46 ("memory channel data switch ... dynamically allocate the at least one multi-use memory channel" and "an arbitration and control engine") at col. 20 lines 27-33 and col. 21 lines 26-43. Apostol also discloses that the integrated circuit 10 is coupled to a display 70 ("a display") at Fig. 2.

6. As per claim 36, Apostol discloses a unified memory system in which the graphics and display subsystem uses the same memory as the processor at col. 1 lines 58-61.

7. As per claims 38, 39, and 43, Apostol discloses that the graphics and display subsystem supports direct attachment to a CRT monitor and the external memory 46 is used to hold video frame buffer at col. 6 line 65-col. 7 line 4 and Fig. 2.

8. As per claim 41, Apostol discloses that the external memory 46 comprises SDRAM at Fig. 2.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. **Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,247,084 to Apostol, Jr., et al and U.S. Patent No. 5,815,167 to Muthal et al.**

12. As per claim 35, Apostol does not expressly teach "a multiplexer configured to selectively couple at least one external memory subsystem to one of the at least one multi-use memory channels". Muthal teaches a system providing concurrent access by a processor and a graphics controller to a shared memory including a frame buffer portion and a main memory portion comprising DRAM rows 220.1 and 220.2. Muthal discloses an arbitration unit 216 for performing an arbitration protocol and granting access using selector means such as multiplexors at col. 6 lines 46-60. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Apostol and Muthal such that a selector

means such as multiplexors are used in Apostol's invention to selectively couple rows or banks of external memory to the system bus 22.

13. **Claims 37 and 42 rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,247,084 to Apostol, Jr., et al and U.S. Patent No. 5,544,306 to Deering et al.**

14. As per claims 37 and 42, Apostol does not expressly teach that the memory sub-systems include a data manipulator containing plural storage elements. Deering teaches a memory chip, FBRAM 71, including a DRAM array comprising four banks and corresponding four page buffers, a pixel buffer, and a pixel ALU at col. 7 lines 27-67 and Fig. 2. Deering further teaches that the pixel ALU comprises a set of raster operation and blend units, a compare unit, and a constant register at col. 15 lines 10-17 and Fig. 8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined the teachings of Apostol and Deering such that the memories of Apostol's invention are implemented with the FBRAM taught by Deering for the purpose of providing a "write-mostly" architecture that minimizes average memory cycle time for overall increase in system performance.

Double Patenting

15. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

16. Claims 34-43 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 34-43 of copending Application No. 10/201492. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of the instant application are broader than the claims of copending application, and therefore claims 34-43 of the copending application include all of the limitations of claims 34-43 of the instant application.

17. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

18. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6295074 to Yamagishi et al.

U.S. Patent No. 6232990 to Poirion

U.S. Patent No. 6215497 to Leung

U.S. Patent No. 6108015 to Cross

U.S. Patent No. 6101584 to Satou et al.

U.S. Patent No. 6081279 to Reddy

U.S. Patent No. 6041400 to Ozcelik et al.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ulka Chauhan** whose telephone number is **(703) 305-9651**. The examiner can normally be reached Mon.-Fri. from 9:00 am to 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

20. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 305-4700.

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
April 3, 2003